



PTO/SB/21 (03-03)
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	10/684,713
	Filing Date	10/14/2003
	First Named Inventor	Paul Arthur Layman
	Art Unit	2811
	Examiner Name	Unassigned
Total Number of Pages in This Submission	Attorney Docket Number	Chaudhry 25-18-8-12-5/075903-282

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance Communication to a Technology Center (TC)
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual	John L. DeAngelis, Jr., Esquire, Reg. No. 30,622 Beusse Brownlee Wolter Mora & Maire, P.A.
Signature	
Date	February 25, 2004

CERTIFICATE OF TRANSMISSION/MAILING	
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231 on this date: 02/25/2004	
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Signature	
Date	02/25/2004

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Paul Arthur Layman, et al**

Group Art Unit: **2811**

Serial No.: **10/684,713**

Examiner: **Unassigned**

Filed: **10/14/2003**

Confirmation No.: **4836**

Atty. Docket No.: **Chaudhry 25-18-8-12-5/075903-282**

For: **Multiple Operating Voltage Vertical Replacement-Gate (VRG) Transistor**

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

- ☒ 1. Pursuant to 37 CFR 1.97(b)
(within 3 months of filing or prior to 1st Office Action)
- ☐ 2. Certification Pursuant to 37 CFR 1.97(c)
(before Final Office Action or Allowance)
- ☐ 3. Fee Payment Pursuant to 37 CFR 1.97(c)
(before Final Office Action or Allowance)
- ☐ 4. Petition, Certification & Petition Fee Payment Pursuant to 37 CFR 1.97(d) (before issue fee payment)

February 25, 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following are submitted in the above identified application in compliance with 37 CFR 1.97 and 1.98:

- ☒ 5. A list of documents on form PTO-1449 together with copies of each identified document and a translation or a concise explanation of each non-English language document is enclosed herewith.

This paper is submitted in accordance with:

- ☒ 6. 37 CFR 1.97(b): [within 3 months of filing or prior to 1st Office Action];
- ☐ 7. 37 CFR 1.97(c): [before Final Office Action or Allowance, whichever is earlier; and
- ☐ 8. The required certification made in item 11 below; or



9. The \$240.00 fee specified in 37 CFR §1.17(p) for submission of this Information Disclosure Statement is authorized in item 14 below.

☐ 10. 37 CFR § 1.95(d): [before issue fee payment]; and

a) This is a petition for consideration of the subject Information Disclosure Statement. The petition fee (\$130.00) required by 37 CFR 1.17(i)(1) is enclosed via check. (Direct this letter to: "Attention PETITIONS EXAMINER" and if applicable include batch locator information: e.g. "Allowed Files, Batch ____, Date of Allowance ____"), and

b) The required Certification is stated in item 11 below.

☐ 11. Certification

☐ 12. Each item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Statement; or

☐ 13. No item of information contained in this Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the person signing this document after making reasonable inquiry, was known to any individual designated in 37 CFR 1.56(c) more than three (3) months prior to the filing of this Statement.

☐ 14. Please charge all applicable fees associated with the submittal of this Information Disclosure Statement to Deposit Account No. _____.

An original and two (2) copies of this document are enclosed.

Respectfully submitted,

John L. DeAngelis, Jr., Esquire
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CERTIFICATE OF MAILING

I HEREBY CERTIFY that this Supplemental Information Disclosure Statement is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 25 day of February, 2004.

Pamela A. Pagel



U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Application Number	10/684,713
Filing Date	10/14/2003
First Named Inventor	Paul Arthur Layman
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Sheet 1 of 2

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Substitute for form 1449/PTO SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)				Complete if Known	
				Application Number	10/684,713
				Filing Date	10/14/2003
				First Named Inventor	Paul Arthur Layman
				Art Unit	2811
				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket Number	Chaudhry 25-18-8-12-5/075903-282

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²	
	1	DUDEK, ET AL, "Lithography-Independent Nanometer Silicon MOSFET's on Insulator", IEEE Transactions on Electron Devices, Vol. 43, No. 10, October 1996, pp. 1626-1631.		
	2	RISCH, ET AL, "Vertical MOS Transistors with 70 nm Channel Length", IEEE Transactions on Electron Devices, Vol. 43, No. 9, September 1996, pp. 1495-1498.		
	3	TAKATO, ET AL, "Impact of Surrounding Gate Transistor (SGT) for Ultra-High-Density LSI's", IEEE Transactions on Electron Devices, Vol. 38, No. 3, March 1991, pp. 573-577.		
	4	TAKATO, ET AL, "High Performance CMOS Surrounding Gate Transistor (SGT) for Ultra High Density LSI's", IEDM 1988, pp. 222-225.		
	5	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", Technical Digest of IEDM, 1999, pp. 75-78.		
	6	OH, ET AL, "50 nm Vertical Replacement-Gate (VRG) pMOSFETs", IEEE 2000.		
	7	HERGENROTHER, ET AL, "The Vertical Replacement-Gate (VRG) MOSFET: A High Performance Vertical MOSFET with Lithography-Independent Critical Dimensions", no publication information apparent from document.		
	8	MONROE, ET AL, "The Vertical Replacement-Gate (VRG) Process for Scalable, General-purpose Complementary Logic", Paper 7.5, pp. 1-7, date and publication information unknown.		

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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